BENEFITS OF FD SOI ADOPTION WITH MIGRATION TO 14NM AND SMALLER FEATURE DIMENSIONS

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IBS White Paper
June 2016

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Overview

The market for semiconductor products continues to require lower costs, lower power consumption, and higher performance, with the integration of a wide range of IP, including processors and memory blocks as well as wireless and wireless connectivity blocks. Semiconductor products are becoming application solutions, which also involves the support of application software as well as key hardware functions.

Planar bulk high-k metal gate (HKMG) CMOS technology is used for a wide range of products, and 28nm HKMG technology will be utilized for many years because of the ability to be cost effective for many applications. The traditional approach in the semiconductor industry has been to periodically reduce feature dimensions, but the benefits of this approach have dissipated because of increasing costs. An example is that there have been major challenges from a power consumption and gate cost perspective with the migration to 20nm HKMG. This technology node is not being used for high-volume production and represents the lower limit of scaling planar bulk CMOS.

There is the ramp-up of high-volume wafers in 16nm and 14nm FinFETs and Intel's Tri-Gate structure. The use of FinFET and Tri-Gate structures gives improvements in power consumption and performance compared to 28nm HKMG bulk CMOS. Gate costs, however, are higher at 16/14nm than at 28nm. The 16/14nm FinFETs and 20nm bulk CMOS represent the first time in the semiconductor industry when a new technology has higher gate cost than the existing technology node.

The semiconductor industry is migrating to 10nm and 7nm. While there will be the ability to have higher performance and lower power consumption compared to 16/14nm, there will be the penalty of higher gate costs.

With the migration to 10nm and 7nm, there will also be a large increase in design implementation costs, which will limit the use of the technology to high-volume applications, where product revenues are 10 times the costs of designing products. The processors for high-end smartphones and data centers can absorb high costs, but many applications continue to utilize older generations of technology rather than migrating to advanced features such as 7nm.

The support of applications such as for IoT also requires the integration of RF and embedded nonvolatile memory functionality. Large cost premiums and substandard high-frequency characteristics are associated with the use of FinFET structures, and as a result, other technology options need to be considered. The semiconductor industry should adopt the best technologies that are appropriate for targeted applications rather than trying to optimize the use of substandard technologies. A viable alternate technology option is FD SOI.

The analysis on wafer cost, gate cost, and transistor cost indicates that 14nm FD SOI has lower costs compared to 16/14nm FinFETs based on the same manufacturing ecosystem. The analysis also indicates that the performance of 14nm FD SOI is comparable to that of 16/14nm FinFETs, and the power consumption of FD SOI can be lower. The result is that 14nm FD SOI can be very competitive with 16/14nm FinFETs for many digital designs and superior to 16/14nm FinFETs for RF-centric IoT and other applications.

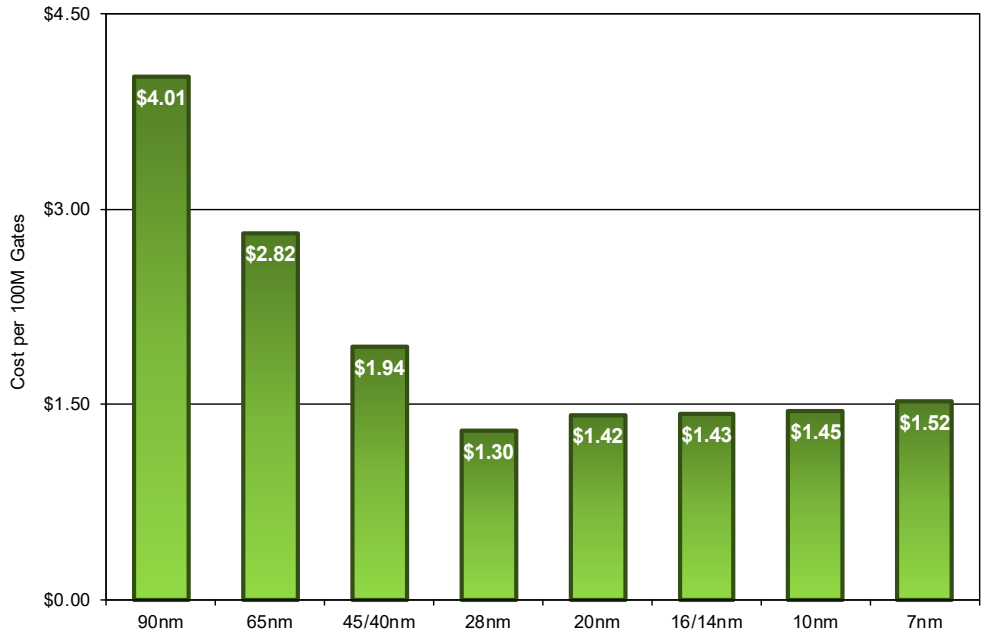
Globalfoundries has established wafer capacity for FD SOI in 22nm while Samsung Electronics and STMicroelectronics have wafer capacity at 28nm FD SOI. There is the expectation that wafer capacity will be established for 14nm FD SOI, and the cost of this wafer capacity should not be high because the same BEOL technology as for 16/14nm FinFETs can be used.

A specific technology node such as 14nm can have high volume use for 30 or more years. The reality is that this technology node is relatively new by the standards of the semiconductor industry. Consequently, there are opportunities to establish alternate wafer processing technologies such as FD SOI that can provide good financial returns for many decades.

Gate Cost Metrics for Different Technology Approaches

A perspective on gate costs with the reduction in feature dimensions is shown in the following figure and table.

FIGURE 1
Gate Cost Trend



Source: International Business Strategies, Inc.

TABLE 1
Gate Cost Trend

Technology	Gates/mm^2 (KU)	Gate utilization (%)	Used gates/mm^2 (KU)	Parametric yield impact (Δ from D_0 yield)	Actual used gates/mm^2 (KU)	Gates/ wafer (MU)	Wafer cost ($)	Wafer cost (Δ)	Cost per 100M gate ($)
90nm	637	86	546	97	532	33,831	1,357.62	--	4.01
65nm	1,109	83	919	96	885	56,330	1,585.71	16.8	2.82
45/40nm	2,139	78	1,677	92	1,538	97,842	1,898.83	19.7	1.94
28nm	4,262	77	3,282	87	2,855	181,658	2,361.84	24.4	1.30
20nm	6,992	65	4,524	73	3,293	209,541	2,981.75	26.2	1.42
16/14nm	10,488	64	6,712	67	4,497	286,140	4,081.22	36.9	1.43
10nm	14,957	60	8,974	62	5,564	354,013	5,126.35	25.6	1.45
7nm	17,085	59	10,080	60	6,048	384,813	5,859.28	14.3	1.52

Note:
* 90nm, 65nm, 45/40nm, 28nm, and 20nm are in two years of high-volume production.
* 16/14nm is in Q4/2016, 10nm is in Q4/2017, and 7nm is in Q4/2018.

The key issues in the gate cost trend include the following:

- The gate cost trend provides visibility into the impact of the migration from planar bulk HKMG CMOS to the adoption of FinFET structures. The data shown assumes the use of high-volume wafer fab facilities that operate at 95% capacity utilization and depreciate over five years. The gate cost is applicable to mainstream wafer manufacturers, with the actual data for feature dimensions being down to 16/14nm and projections for 10nm and 7nm.

- The increase in gate cost at 20nm bulk HKMG CMOS has resulted in this technology having a short lifetime, with relatively few designs being implemented at this technology node. The 20nm HKMG bulk CMOS also has high leakage and higher power consumption compared to 28nm HKMG bulk CMOS, which has limited its use within mobile applications.

  Globalfoundries has developed its 22nm FD SOI technology, which obsoletes 20nm bulk HKMG CMOS for digital, mixed-signal, and RF functionality. The 22nm FD SOI technology of Globalfoundries is also expected to make 28nm HKMG bulk CMOS technology obsolete for many products.

- The increase in gate cost at 16/14nm has relegated this technology to a relatively small number of designs. However, there is high-volume production for processors for smartphones and notebook computers because of the need for low power consumption and relatively high performance. There has been the willingness to pay price premiums in order to get the reduction in power consumption and higher performance for higher-end smartphones.

- The 10nm technology node is expected to have a short time window within the foundry ecosystem because 7nm will likely be available 12 months after the 10nm technology node. The strategies of mainstream foundry vendors are to bring up 7nm into high-volume production in 2018.

  The 7nm technology node is expected to be used for several years because 5nm will need to use EUV lithography for multiple layers, and there is some uncertainty regarding the timing of when EUV will be cost competitive for high-volume production. Samsung is planning to use EUV for 7nm. However, if EUV is not ready when expected, Samsung could use 193nm lithography.

  There is the migration to 7nm FinFET because this is the best option that is available within the mainstream market. It is also appropriate to evaluate other options.

- There are concerns that FD SOI is a high-cost technology. A perspective on the costs for manufacturing 16/14nm FinFET and 14nm FD SOI wafers is shown in the following table.

TABLE 2
Wafer Costs

	16/14nm FinFET		14nm FD SOI	
	$	%	$	%
Depreciation	2,303.94	58.79	1,972.26	53.24
Equipment maintenance	581.42	14.84	445.32	12.02
Direct labor	64.78	1.65	45.52	1.23
Indirect labor	238.76	6.09	208.36	5.62
Facilities	232.47	5.93	189.37	5.11
Wafer cost	99.93	2.55	475.00	12.82
Consumables	359.28	9.17	331.47	8.95
Monitor wafers	38.62	0.99	37.24	1.01
TOTAL Unyielded wafer cost	3,919.20	100.00	3,704.54	100.00
Line yield (%)	96.03	--	97.96	--
TOTAL Yielded wafer cost	4,081.22	--	3,781.69	--

The analysis shows the wafer cost of 14nm FD SOI is 7.3% lower than that of 16/14nm FinFETs. The most important factor in the lower cost is the smaller number of masking steps for FD SOI. The lower number of mask steps will also shorten the cycle time of wafer fabs for FD SOI wafers.

While wafer cost is important, a more important factor for the users of wafers is gate cost. A perspective on these costs is shown in the following table.

TABLE 3
Comparison of Wafer Costs and Gate Costs

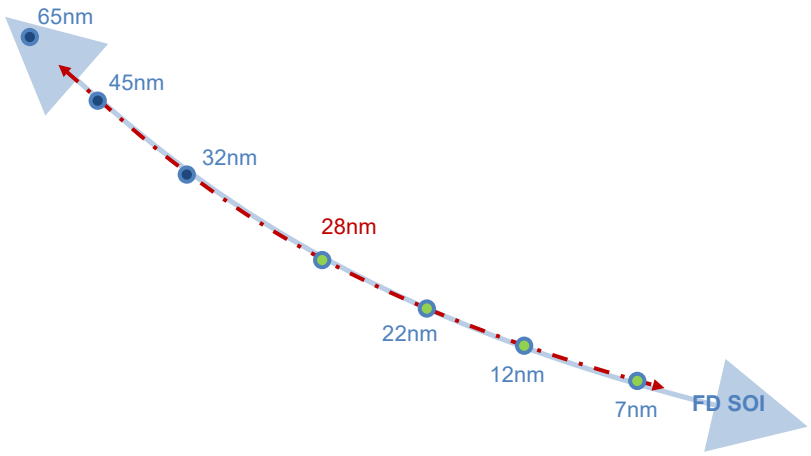
($)	Wafer cost	Gate (100M) cost
16/14nm FinFET	4,081.22	1.43
14nm FD SOI	3,781.69	1.19

The gate cost is analyzed based on the combination of wafer cost, chip size, and product yield. The assumption is that chip size is comparable between these two technologies, but 14nm FD SOI has 10% higher yield than 16/14nm FinFETs. The gate cost for 14nm FD SOI is 16.6% lower than that for 16/14nm FinFETs, with comparable wafer fab metrics. This is only a large cost difference and represents a major competitive advantage for FD SOI.

Due to the lower gate cost and ability to support RF functionality for IoT and other applications, 14nm FD SOI is a superior technology compared to 16/14nm FinFETs for many applications. Even though 16/14nm FinFETs is in high-volume production, the expectation is that there is a window of opportunity for 14nm FD SOI.

It is projected that FD SOI can scale to 7nm, and a perspective is provided by CEA-Leti.

FIGURE 2
Scaling of FD SOI to 7nm



Leti @ 7nm

Modeling
Boosters: Gate last, sSOI, strain, Ge
Early design

FD SOI is extendable up to 7nm

Strain maximizes energy efficiency/FinFET (increase current WO increasing capacity)

Back bias: 2X stronger @ 7nm/22nm

Source: CEA-Leti

The result of potentially scaling to 7nm means that FD SOI can support multiple technology nodes and is expected to have a useful lifetime of 30 or more years.

Key issues are which company will take the lead in establishing large wafer fab capacity for 14nm FD SOI and which customers will implement designs with this technology.

Market Potential for 28nm, 22/20nm, and 14nm FD SOI

The foundry market by technology node for 28nm, 22/20nm, and 16/14nm is shown in the following figure and table.

FIGURE 3
Foundry Market for 28nm, 22/20nm, and 16/14nm

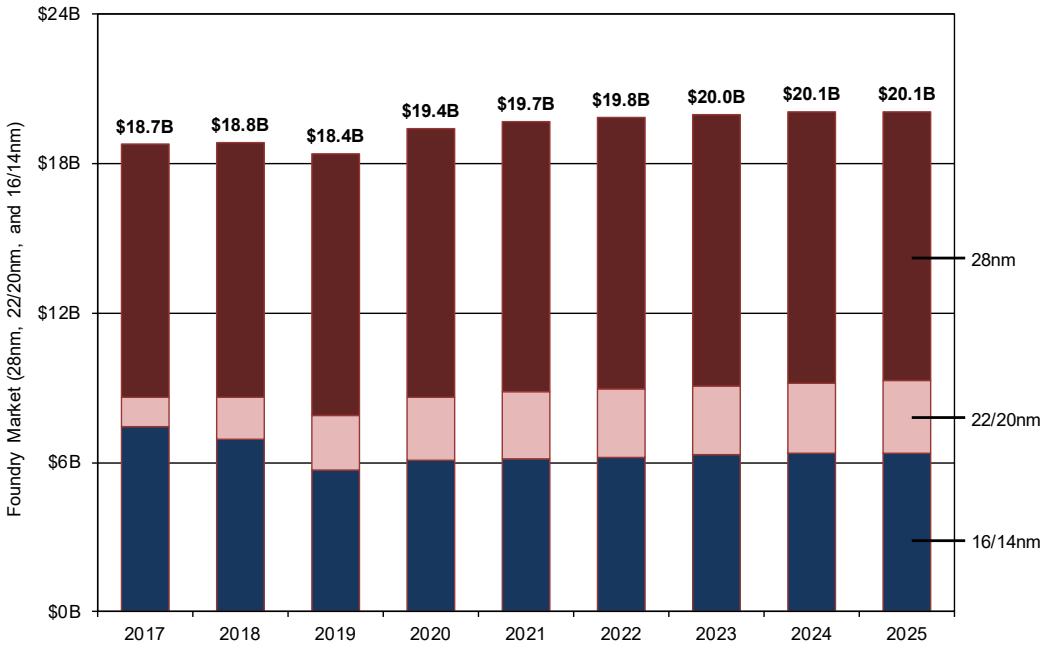


TABLE 4
Foundry Market for 28nm, 22/20nm, and 16/14nm

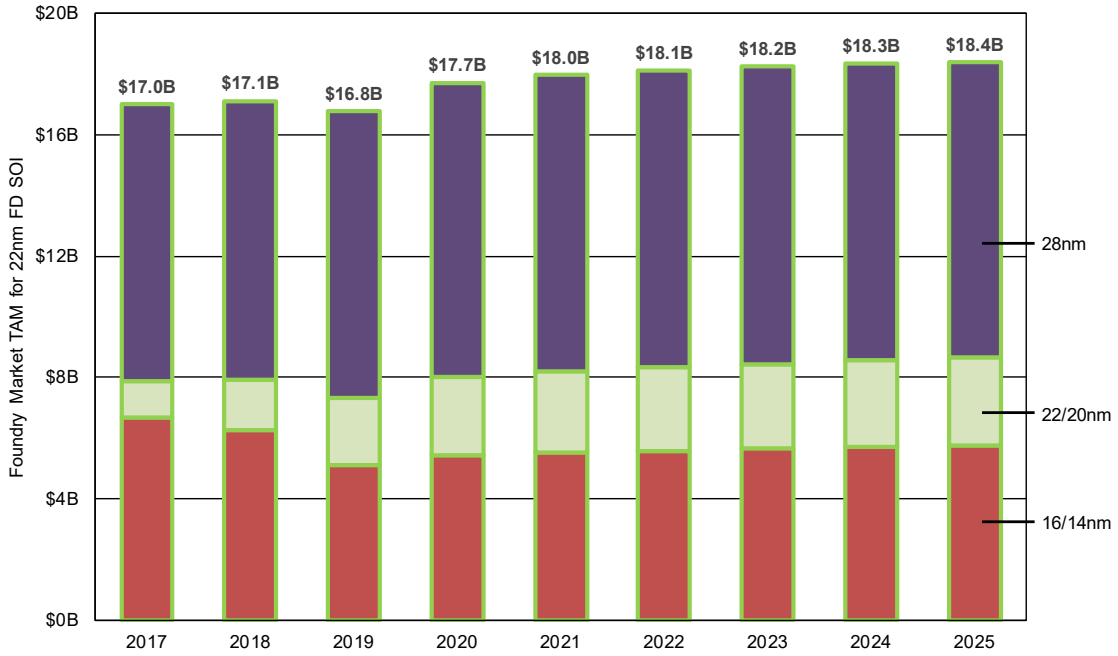
	2017	2018	2019	2020	2021	2022	2023	2024	2025
16/14nm ($M)	**7,434**	**6,955**	**5,673**	**6,059**	**6,144**	**6,218**	**6,286**	**6,343**	**6,387**
Growth rate (%)	NA	(6.4)	(18.4)	6.8	1.4	1.2	1.1	0.9	0.7
Percent total (%)	39.7	36.9	30.9	31.2	31.3	31.4	31.5	31.6	31.8
22/20nm ($M)	**1,192**	**1,661**	**2,203**	**2,546**	**2,671**	**2,735**	**2,792**	**2,848**	**2,902**
Growth rate (%)	NA	39.3	32.6	15.6	4.9	2.4	2.1	2.0	1.9
Percent total (%)	6.4	8.8	12.0	13.1	13.6	13.8	14.0	14.2	14.4
28nm ($M)	**10,120**	**10,215**	**10,506**	**10,802**	**10,845**	**10,878**	**10,889**	**10,867**	**10,802**
Growth rate (%)	NA	0.9	2.8	2.8	0.4	0.3	0.1	(0.2)	(0.6)
Percent total (%)	54.0	54.2	57.2	55.7	55.2	54.9	54.5	54.2	53.8
TOTAL ($M)	**18,746**	**18,831**	**18,382**	**19,407**	**19,660**	**19,831**	**19,967**	**20,058**	**20,091**
Growth rate (%)	NA	0.5	(2.4)	5.6	1.3	0.9	0.7	0.5	0.2

The key conclusions from the analysis of designs within the foundry market indicate the following:

- The foundry market data is provided for 2017 to 2025.
- The analysis of design activities at 28nm HKMG bulk CMOS indicates that all these designs can be addressed by 28nm and 22nm FD SOI. There can be power consumption and performance advantages from using FD SOI rather than HKMG bulk CMOS. It is also likely that some of the 40nm market can be addressed by FD SOI, but this is not factored into the provided data.
- The analysis also indicates that the market for 22/20nm can be addressed by 22nm FD SOI. The reality is that most of the value of this technology is based on Globalfoundries' 22nm FD SOI.
- The analysis of designs in 16/14nm FinFETs indicates that 90% can be addressed by 22nm FD SOI. In the 2019 to 2020 time frame, it is also likely that a significant percentage of 7nm FinFET designs can be addressed by 14nm FD SOI.

As a result of the analysis, the foundry market that can be addressed by FD SOI is shown in the following figure.

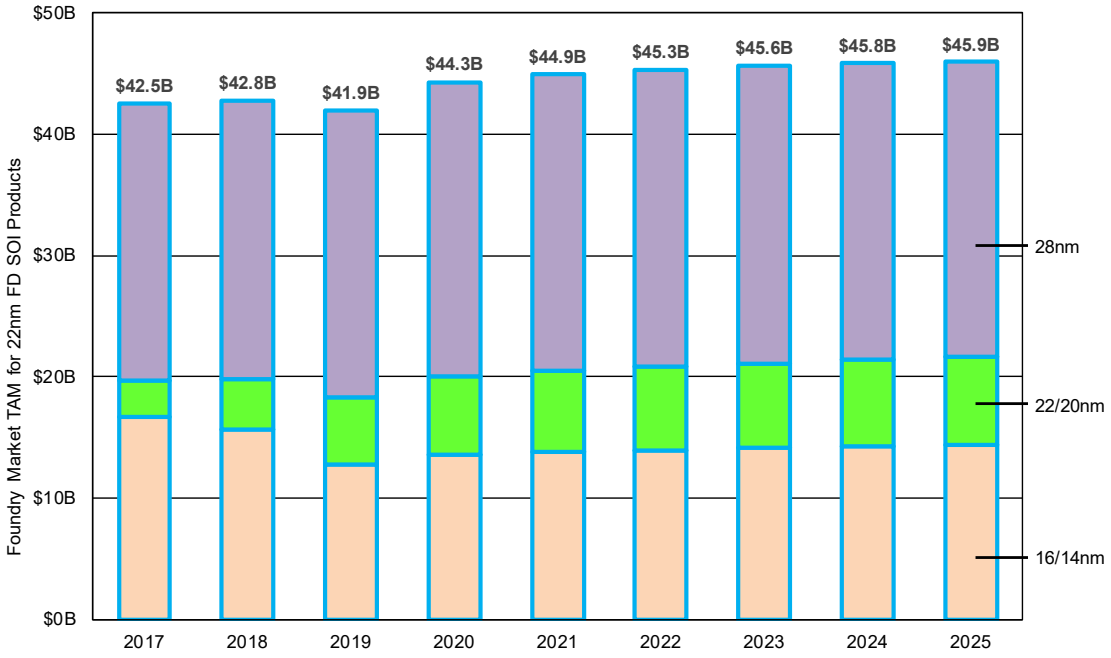
FIGURE 4
Potential Market FD SOI



The TAM for the FD SOI foundry market is projected to be $18.4B in 2025.

The product market (based on cost metrics) is approximately 2.5 times the foundry market. The potential product-based market for FD SOI is projected to be $45.9B in 2025, and this is shown in the following figure.

FIGURE 5
Product Market Value Based on FD SOI



The TAM for FD SOI products is large. With the inclusion of 7nm designs that can be addressed by 14nm FD SOI, the total TAM for FD SOI products can potentially be over $50B in 2025.

A number of specific products and applications can be addressed by FD SOI, including the following:

- ***Advanced driver assistance systems (ADAS).*** The soft-error immunity of FD SOI is superior to other technologies, and this is important in automotive security.
- ***ISP.*** There is the ability to provide high performance with low power consumption.
- ***IoT.*** There is the ability to support ultra-low-power embedded RF connectivity.

The market opportunities for FD SOI are large, but there will be the need for a strong design enablement ecosystem in order to displace various generations of FinFET technology.

FD SOI can be very cost competitive, and the market potential is large. The key issue is which companies will try to be early in the market with new products where they can gain competitive advantages in cost, power consumption, and performance against the established FinFET-based ecosystem.

There can also be the approach of having complementary capabilities between FinFETs and FD SOI. With a common BEOL technology, the financial returns from supporting both technology options can be extensive.

AUTHOR BIOGRAPHY

Dr. Handel Jones is the founder and CEO of International Business Strategies, Inc. (IBS), which is based in Los Gatos (California) and has been in business for over 25 years. IBS is active in quantifying the cost of implementing and manufacturing IC products and financial metrics related to market positioning. IBS provides support to many global leaders in key areas of technologies, markets, and business strategies for the semiconductor and electronics industries.

Dr. Jones is the author of *Chinamerica*, which was published by McGraw-Hill and provides insight into the drivers for the economy of the U.S. and China. As a follow-on to *Chinamerica*, Dr. Jones has recently written a new book called *China's Globalization: How China Can Become No. 1*. In addition, Dr. Jones has contributed to a number of publications, including Wall Street Journal, New York Times, Economist, Reuters, Forbes, China Daily, Global Times, Nikkei Weekly, and others.